AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-functional device comprising:

a bus;

a random access memory (RAM) coupled to said bus;

a central processing unit (CPU) coupled to said bus; and

a plurality of analog blocks coupled to said bus, wherein said bus, RAM, CPU and analog blocks reside on a single chip ~~in a single integrated circuit~~;

said plurality of analog blocks comprising a first set of analog blocks that is ~~can be~~ selectively and electrically couplable ~~coupled~~ to and decouplable ~~decoupled~~ from another analog block in said plurality of analog blocks;

wherein said analog blocks are selectively and electrically coupled to implement a particular analog function, wherein different analog functions are implemented by electrically coupling different combinations of said analog blocks.

2. (Original) The multi-functional device of Claim 1 wherein said first set of analog blocks comprises switched capacitor blocks.

3. (Original) The multi-functional device of Claim 1 wherein said first set of analog blocks comprises a first type and a second type, wherein said first type is adapted to receive a first set of inputs and wherein said second type is adapted to receive a second set of inputs different from said first set of inputs.

4. (Original) The multi-functional device of Claim 1 wherein said plurality of analog blocks also comprises a second set of analog blocks, wherein said second set of analog blocks comprises continuous time blocks.

5. (Original) The multi-functional device of Claim 1 wherein said plurality of analog blocks is arranged in an array having multiple columns and multiple rows.

6. (Original) The multi-functional device of Claim 5 wherein said array comprises a first row of continuous time blocks and multiple rows of switched capacitor blocks, wherein said first row is disposed between a row of switched capacitor blocks and an edge of said array.

7. (Original) The multi-functional device of Claim 5 wherein each analog block in a column is coupled to a respective digital bus.

8. (Original) The multi-functional device of Claim 1 wherein an analog block comprises a plurality of analog elements having changeable characteristics, wherein a characteristic of an analog element is specified according to said particular analog function.

9. (Currently Amended) A method for implementing multiple functions in a device, said method comprising ~~the steps of~~:

[[a)]] selecting a first analog block from a plurality of analog blocks coupled to a bus, a random access memory and a central processing unit on a single chip ~~in a single integrated circuit~~, wherein said first analog block

is ~~can be~~ electrically couplable ~~coupled~~ to and decouplable ~~decoupled~~ from another analog block; and

[[b)]] coupling electrically said first analog block to another analog block to implement a first analog function;

wherein different analog functions are implemented by selectively and electrically coupling different combinations of analog blocks.

10. (Original) The method of Claim 9 wherein said first analog block is a switched capacitor block.

11. (Original) The method of Claim 9 wherein said plurality of analog blocks comprises a plurality of switched capacitor blocks of a first type and a second type, wherein said first type is adapted to receive a first set of inputs and wherein said second type is adapted to receive a second set of inputs different from said first set.

12. (Original) The method of Claim 9 wherein said plurality of analog blocks comprises a plurality of continuous time blocks.

13. (Original) The method of Claim 9 wherein said analog blocks are arranged in an array having multiple columns and multiple rows.

14. (Original) The method of Claim 13 wherein said array comprises a first row of continuous time blocks and multiple rows of switched capacitor blocks, wherein said first row is disposed between a row of switched capacitor blocks and an edge of said array.

15. (Original) The method of Claim 13 wherein each analog block in a column is coupled to a respective digital bus.

16. (Currently Amended) The method of Claim 9 comprising ~~the step of~~:

[[c)]] changing a characteristic of an analog element of said first analog block, wherein said characteristic is specified according to which analog function is being implemented.

17. (Currently Amended) An array of analog blocks comprising:

a first plurality of analog blocks comprising continuous time blocks; and

a second plurality of analog blocks comprising switched capacitor blocks, said second plurality of analog blocks coupled to said first plurality of analog blocks, wherein a switched capacitor block is ~~can be~~ selectively and electrically couplable ~~coupled~~ to and decouplable ~~decoupled~~ from another analog block;

wherein said first plurality and said second plurality of analog blocks are selectively and electrically coupled in different combinations to implement different analog functions, and wherein said first plurality and second plurality of analog blocks are coupled to a bus, a random access memory and a central processing unit on a single chip.

18. (Original) The array of analog blocks of Claim 17 wherein said switched capacitor blocks comprise a first type and a second type, wherein

said first type is adapted to receive a first set of inputs and wherein said second type is adapted to receive a second set of inputs different from said first set.

19. (Original) The array of analog blocks of Claim 17 wherein said array comprises a first row of continuous time blocks and multiple rows of switched capacitor blocks, wherein said first row is disposed between a row of switched capacitor blocks and an edge of said array.

20. (Original) The array of analog blocks of Claim 19 wherein each analog block in a column is coupled to a respective digital bus.

21. (Original) The array of analog blocks of Claim 17 wherein an analog function is an amplifier function, a digital-to-analog converter function, an analog-to-digital converter function, an analog driver function, a low band pass filter function, or a high band pass filter function.

22. (Original) The array of analog blocks of Claim 17 wherein an analog block comprises a plurality of analog elements having changeable characteristics, wherein a characteristic of an analog element is specified according to said particular analog function.